nents with registers clocked as a direct result of input data to aid in explaining the rationale of one illustrative embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1, which shows the basic arrangement having a computer 10 and a software protection security device 12 being connected to a port of the computer via an interfacing connector 14 which permits the communication between the computer 10 and the hardware security device 12. The interface connector 14 includes a plurality of lines 16 for transmitting a plurality of bits from the computer to the security device 12. The interconnector 14 also contains a line 18 through which a signal of acknowledgement is provided. The signals sent to the security device in the form of bits are generally under control of a specific software program running in the computer whereas the signals returning from the security device 12 are in response to the signals transmitted thereto from the computer. If the signals from the security device 12 in response to those from the computer are determined by the software as being proper and correct, it is then generally assumed that a proper security device has been connected to that computer port. The vulnerability of the system illustrated in FIG. 1 resides in the interface connector 14 which may be tapped and the signals to and from the security device 12 can be monitored, studied and by the application of reverse engineering, the operation of the security device can be broken and emulated.

In accordance with the present invention a disguised predetermined control code which is sent over the lines 16 of the interconnector 14 is compared with a stored reference code, and decoded in apparatus which is incorporated and contained in the security device 12. The predetermined control code has no special attributes over any other random signal and could only be determined and used in the decoder, accordingly rendering detection of the internally coded signals by an ordinary means of observation impossible. The stored reference code inclusive in the security device is not the same as, and should not be confused with the disguised predetermined control code required to cause the security device to respond. The stored reference cod in the security device 12 may be altered by means of apparatus either directly or indirectly as a result of signals from the computer under the command from software which is operating the computer and which is desired to be protected. The everchanging local stored reference code although predetermined by the programmer when intermixed with the other signals appearing as bits on the interconnector line 16 would appear to be completely random to an outside observer since the true disguised predetermined reference code cannot be distinguished from any other series of signals which are fed to the security device and need appear no more frequently than would occur if they were part of a truly random sequence. Thus, in accordance with the present invention the security of the system will lie in the fact that no logical sequence exists in a totally random field making the apparatus extremely difficult to reverse engineer. Both the control code and the reference code are of necessity sequentially varied using the same sequence for both.

Referring first to FIG. 2, apparatus and its several variants will be described for coding and decoding signals applied to the security device 12 in which the apparatus acts as a digital filter which provides an output when the input signals match a given reference in accordance with digital logic convention. For example, in FIG. 2A, a simple logical AND gate 22 is shown having an input 20 and a reference input 23. When the reference input 23 is at logic 1, an output 24 will be a true logic 1 when an input 20 matches its reference 23. Similarly, in FIG. 2B which illustrates a logical NOR gate 25 provides an output 28 which is a logical 1 when the input 26 matches the reference input 27 at a logical 0. These types of output become analagous to a high and a low pass single bit filter in FIGS. 2A and 2B, respectively. It will be appreciated that the filter does not pass anything but simply indicates a match whenever there is a high or a low bit present at the input of the logical gate.

FIG. 2C illustrates the combination of the high and low bit filters by means of an AND gate 29 and a NOR gate 30 each having common input 32 and a common reference input 33 whose respective outputs are applied to the input of an OR gate 31. The output 34 of the OR gate 31 is a true logic 1 whenever the input level 32 matches the reference level 33, and accordingly, by selecting a given reference, a single bit level may thus be filtered. In FIG. 2D, a schematic representation is shown of an EXCLUSIVE NOR gate which is the logical equivalent of the circuit shown in FIG. 2C. An EXCLUSIVE NOR gate 35 has an input 36 and a reference input 37 applied thereto and an output 38 is provided whenever the input 36 matches reference input 37 thereby producing a logical 1 at the output 38. An EXCLUSIVE OR gate can be used when selecting the complement of the EXCLUSIVE NOR gate. In view of the simplicity and versatility of the EXCLUSIVE NOR gate 35, it will be used in explaining the present invention in preference to other configurations illustrated in FIG. 2. However, it should be apparent to those skilled in the art that such a preference is not considered to limit the present invention to the chosen illustrations as other filters may be utilized depending on the particular application and the effect desired. In addition, it should be pointed out that for purposes of discussion although positive logic convention may be used for illustrative purposes, it is equivalent to negative logic convention and further, anyone skilled in the art may, for convenience or otherwise, combine both types of logic convention for a given design application. Failure to illustrate all the variances due to specific logic elements should not be considered limitations on the scope of the present invention.

Referring now to FIG. 3A, an implementation of the present invention is illustrated using an EXCLUSIVE NOR gate of the type illustrated in FIG. 2D. In FIG. 3 EXCLUSIVE NOR gates 44 and 49 are illustrated and the exact number of EXCLUSIVE NOR gates utilized will depend on the number of bits 43 supplied from different lines from the computer. Each EXCLUSIVE NOR gate is supplied with a memory cell namely, memory 41 for EXCLUSIVE NOR gate 44, and memory 48 for EXCLUSIVE NOR gate 49. Each memory cell will provide the reference for its respective bit which is transmitted via the line 16 of the connector 14 from the computer 10. The memory cells 41 and 48 may be any means which provide provide one state or another including hand wiring the reference input to a high or a low which is the simplest form, or may comprise a more sophisticated electrically programmable cell. As illus-